



ESDA25DB3

Application Specific Discretets
A.S.D.™

TRANSIL ARRAY FOR ESD PROTECTION

APPLICATIONS

Where transient overvoltage protection in esd sensitive equipment is required, such as :

- COMPUTERS
- PRINTERS
- COMMUNICATION SYSTEMS

It is particularly recommended for RS232 I/O port protection where the line interface withstands 2 kV, ESD surges.

FEATURES

- 18 BIDIRECTIONAL TRANSIL FUNCTIONS
- LOW CAPACITANCE : $C = 30\text{pF} @ V_{RM}$
- 500 W peak pulse power (8/20 μs)

DESCRIPTION

The ESDA25DB3 is a dual monolithic voltage suppressor designed to protect components which are connected to data and transmission lines against ESD.

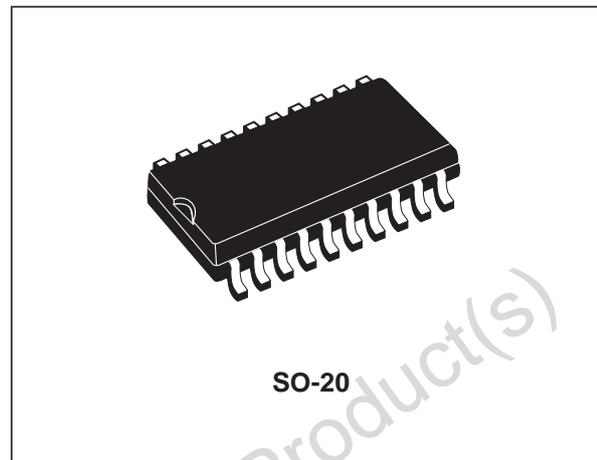
BENEFITS

High ESD protection level : up to 25 kV
High integration
Suitable for high density boards

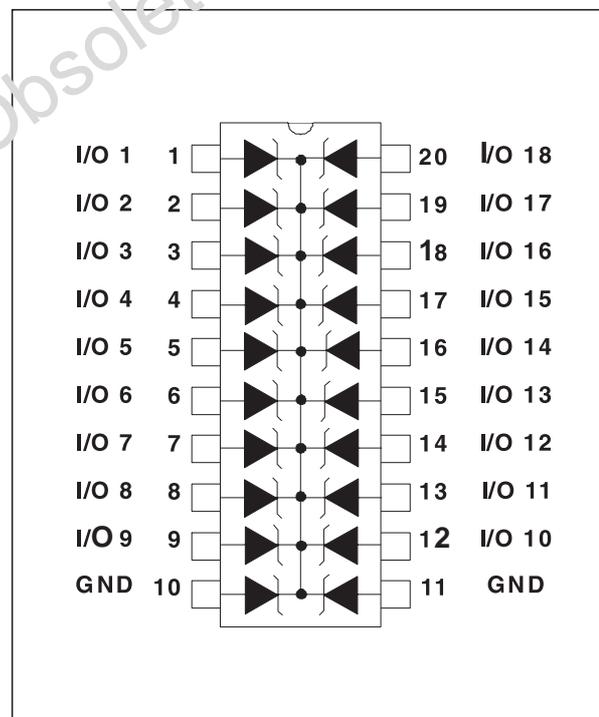
COMPLIES WITH THE FOLLOWING STANDARDS :

IEC 1000-4-2 : level 4

MIL STD 883C-Method 3015-6 : class 3
(human body model)



FUNCTIONAL DIAGRAM



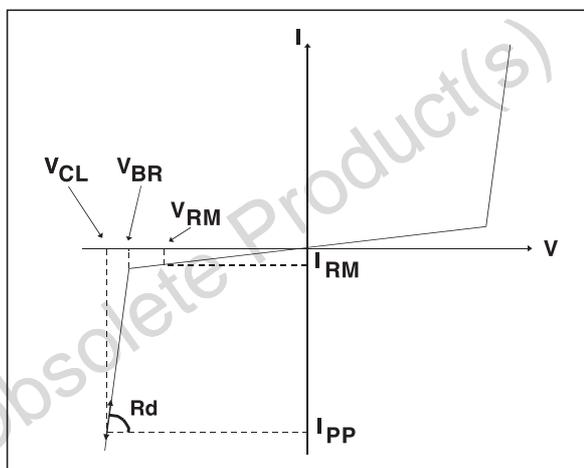
ESDA25DB3

ABSOLUTE MAXIMUM RATINGS ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter	Value	Unit
V_{PP}	Electrostatic discharge MIL STD 883C - Method 3015-6	25	kV
P_{PP}	Peak pulse power (8/20 μs)	500	W
T_{stg} T_j	Storage temperature range Maximum junction temperature	- 55 to + 150 125	$^{\circ}\text{C}$ $^{\circ}\text{C}$
T_L	Maximum lead temperature for soldering during 10s	260	$^{\circ}\text{C}$

ELECTRICAL CHARACTERISTICS ($T_{amb} = 25^{\circ}\text{C}$)

Symbol	Parameter
V_{RM}	Stand-off voltage
V_{BR}	Breakdown voltage
V_{CL}	Clamping voltage
I_{RM}	Leakage current
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance



Types	V_{BR} @ I_R		I_{RM} @ V_{RM}	R_d	αT	C		
	min.	max.						
	note1							
	V	V	mA	μA	V	Ω	$10^{-4}/^{\circ}\text{C}$	pF
ESDA25DB3	25	30	1	2	24	0.5	9.7	50

note 1 : Between any I/O pin Ground

note 2 : Square pulse, $I_{pp} = 25\text{A}$, $t_p = 2.5\mu\text{s}$.

note 3 : $\Delta V_{BR} = \alpha T * (T_{amb} - 25^{\circ}\text{C}) * V_{BR}(25^{\circ}\text{C})$

CALCULATION OF THE CLAMPING VOLTAGE

USE OF THE DYNAMIC RESISTANCE

The ESDA family has been designed to clamp fast spikes like ESD. Generally the PCB designers need to calculate easily the clamping voltage V_{CL} . This is why we give the dynamic resistance in addition to the classical parameters. The voltage across the protection cell can be calculated with the following formula:

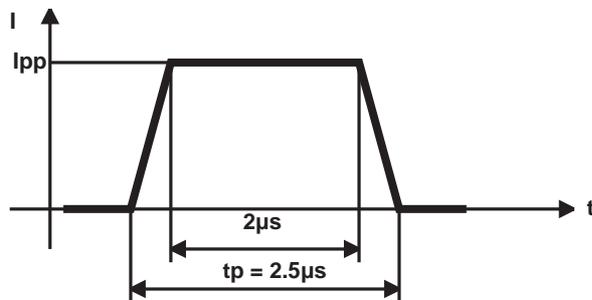
$$V_{CL} = V_{BR} + R_d I_{PP}$$

Where I_{PP} is the peak current through the ESDA cell.

As the value of the dynamic resistance remains stable for a surge duration lower than $20\mu s$, the $2.5\mu s$ rectangular surge is well adapted. In addition both rise and fall times are optimized to avoid any parasitic phenomenon during the measurement of R_d .

DYNAMIC RESISTANCE MEASUREMENT

The short duration of the ESD has led us to prefer a more adapted test wave, as below defined, to the classical 8/20 μs and 10/1000 μs surges.



2.5 μs duration measurement wave.

Fig. 1 : Peak power dissipation versus initial junction temperature.

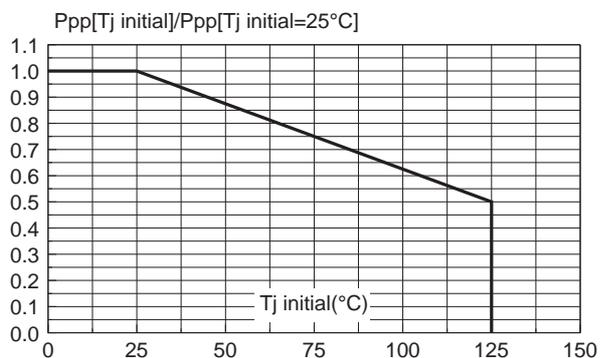


Fig. 2 : Peak pulse power versus exponential pulse duration ($T_j \text{ initial} = 25^\circ\text{C}$).

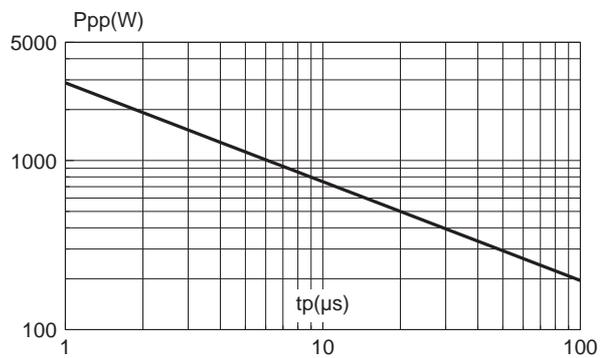


Fig. 3 : Clamping voltage versus peak pulse current ($T_j \text{ initial} = 25^\circ\text{C}$).

Rectangular waveform $t_p = 2.5 \mu\text{s}$.

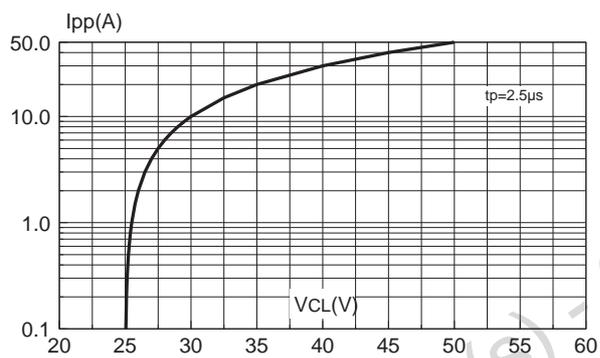


Fig. 4 : Capacitance versus reverse applied voltage (typical values).

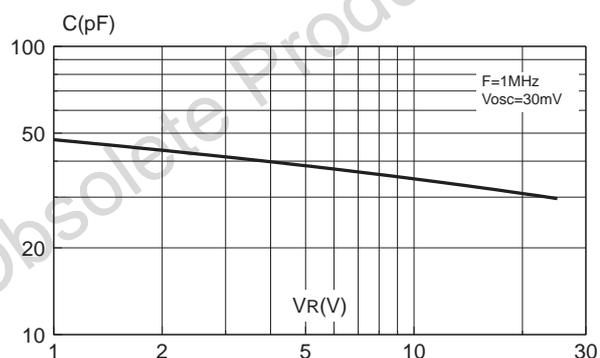
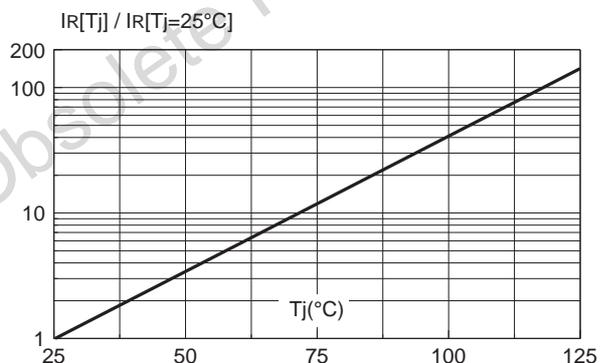
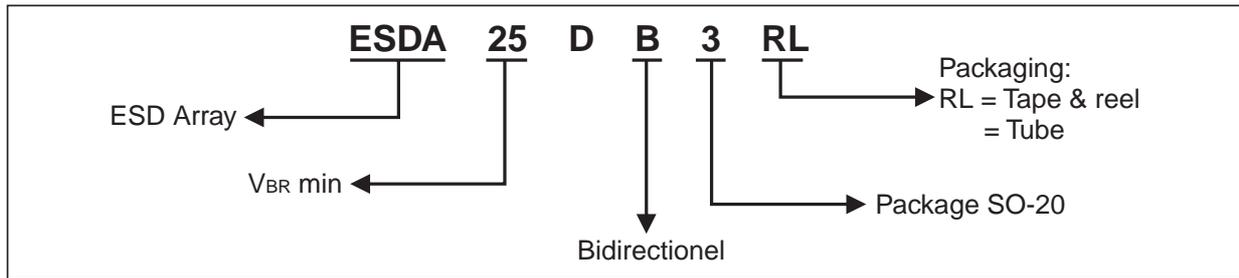


Fig. 5 : Relative variation of leakage current versus junction temperature (typical values).

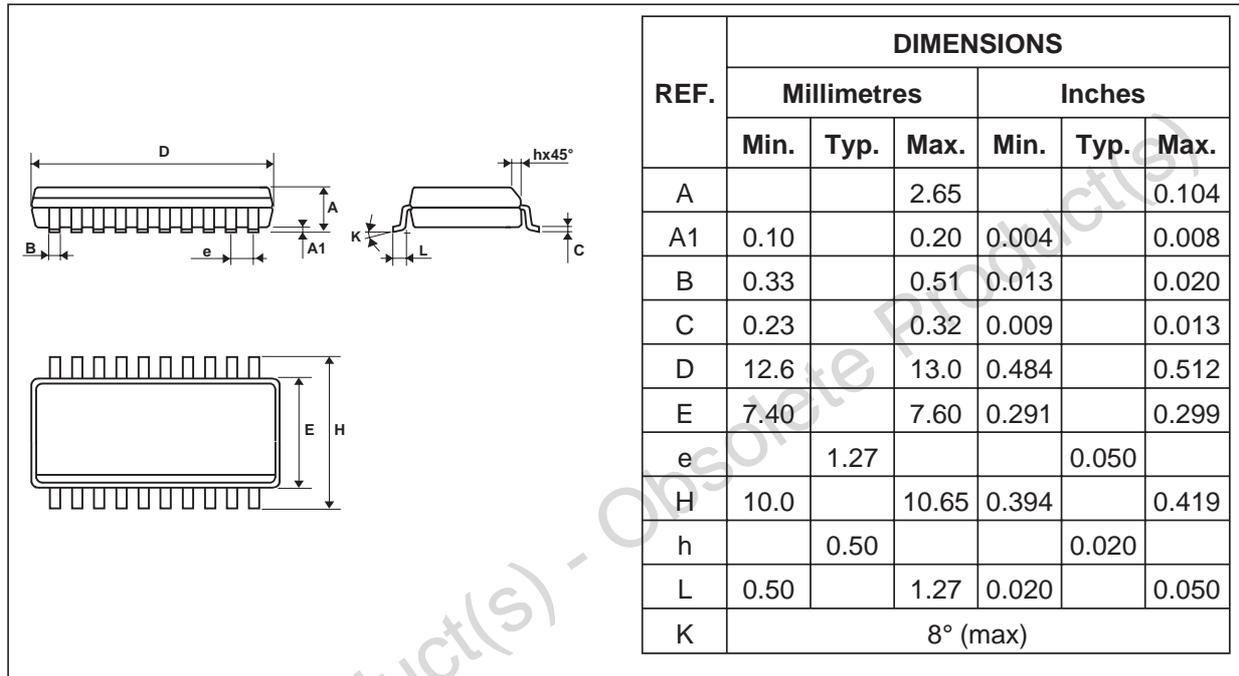


ORDER CODE



PACKAGE MECHANICAL DATA

SO-20 Plastic



Marking: Logo, Date Code, E25DB3

Packaging: Preferred packaging is tape and reel.

Weight: 0.55g.

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