ESDA14V2-2BF3

Quad bidirectional Transil™ array for ESD protection

Features

- 2 bidirectional Transil functions
- ESD protection: IEC 61000-4-2 level 4
- Stand off voltage: 12 V Min.
- Low leakage current
- Very small PCB area < 1.5 mm^2
- 400 microns pitch

Complies with the following standards

- IEC 61000-4-2
  - 15 kV (air discharge)
  - 8 kV (contact discharge)
- MIL STD 883E- Method 3015-7: class 3
  - 25 kV (human body model)

Applications

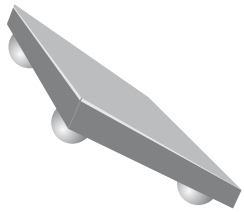
Where transient overvoltage protection in ESD sensitive equipment is required, such as:

- Computers
- Printers
- Communication systems and cellular phones
- Video equipment

Description

The ESDA14V2-2BF3 is a monolithic array designed to protect 2 lines against ESD transients. The device is ideal for applications where both reduced line capacitance and board space saving are required.

This device is particularly adapted to the protection of symmetrical signals.



Flip Chip
(4 bumps)

Figure 1. Pin layout (bump side)

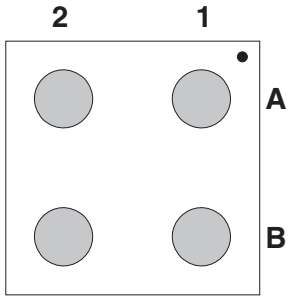
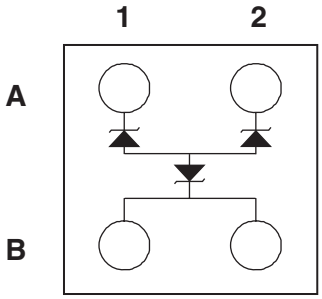


Figure 2. Configuration



TM: Transil is ASD a trademark of STMicroelectronics.

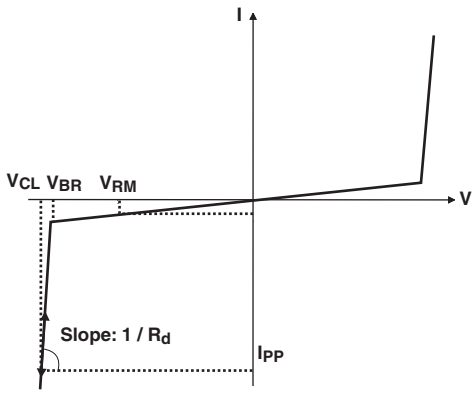
1 Characteristics

Table 1. Absolute ratings (limiting values)

Symbol	Parameter		Value	Unit
V_{PP}	ESD discharge	MIL STD 883E - Method 3015-7 IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge	± 25 ± 15 ± 8	kV
P_{PP}	Peak pulse power (8/20µs)		50	W
T_j	Junction temperature		125	°C
T_{stg}	Storage temperature range		-55 to +150	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C
T_{op}	Operating temperature range		-40 to +125	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
αT	Voltage temperature coefficient
C	Capacitance



Order code	V_{BR} @ I_R			I_{RM} @ V_{RM}		Rd	αT	C
	min.	max		max.		typ.(1)	max.(2)	max. 0 V bias
	V	V	mA	µA	V	Ω	10^{-4}/C	pF
ESDA14V2-2BF3	14.2	18	1	0.5 0.1	12 3	3.2	6.5	12

1. Square pulse, I_{pp} = 3 A, t_p = 2.5 µs.
2. $\Delta V_{BR} = \alpha T^* (T_{amb} - 25\ °C) * V_{BR}$ (25 °C)

Figure 3. Relative variation of peak pulse power versus intial junction temperature

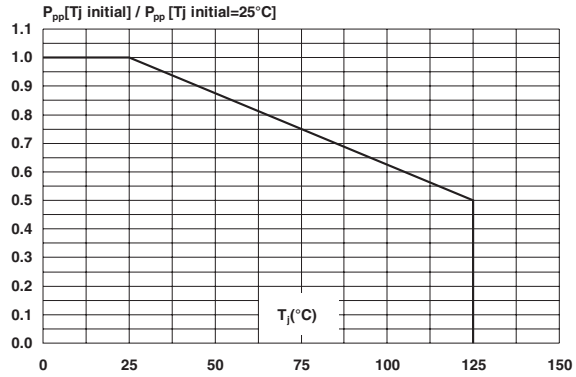


Figure 4. Peak pulse power versus exponential pulse duration

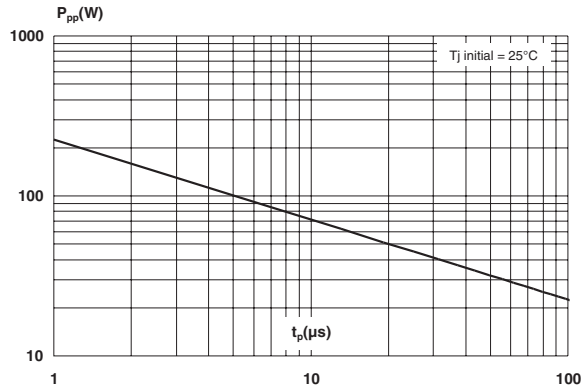


Figure 5. Clamping voltage versus peak pulse current (typical values, rectangular waveform)

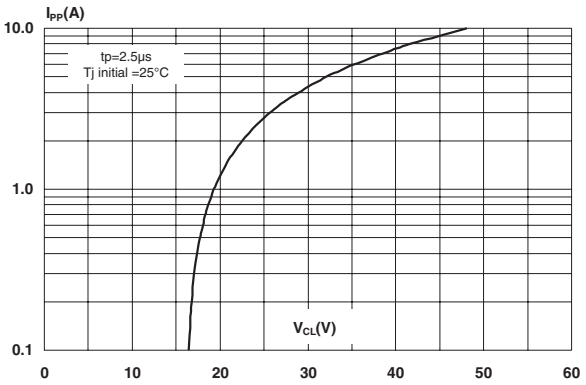


Figure 6. Junction capacitance versus reverse applied voltage (typical values)

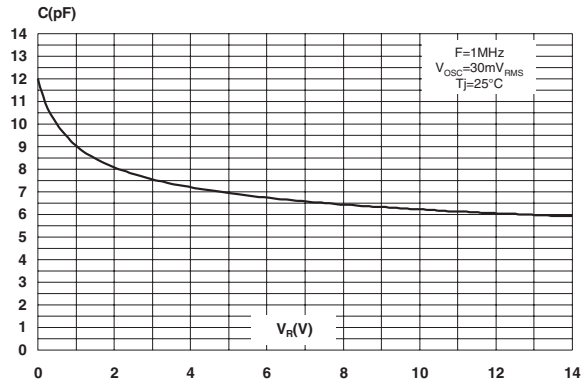


Figure 7. Relative variation of leakage current versus junction temperature (typical values)

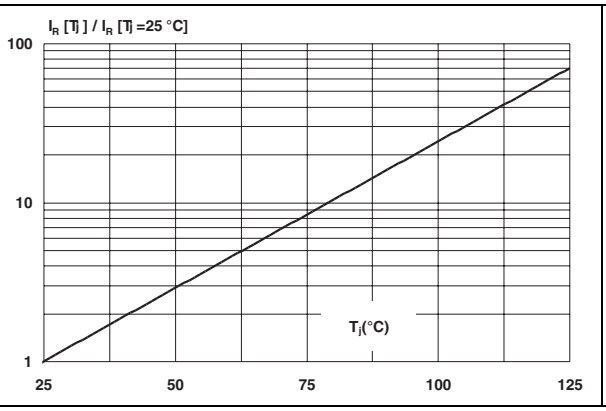


Figure 8. Analog crosstalk measurement

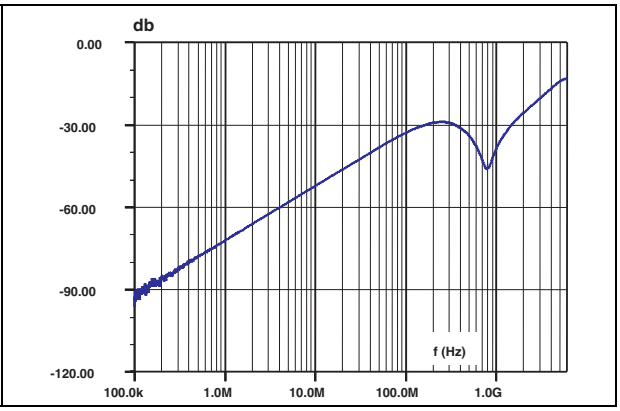


Figure 9. ESD response to IEC 61000-4-2 (+15 kV air discharge)

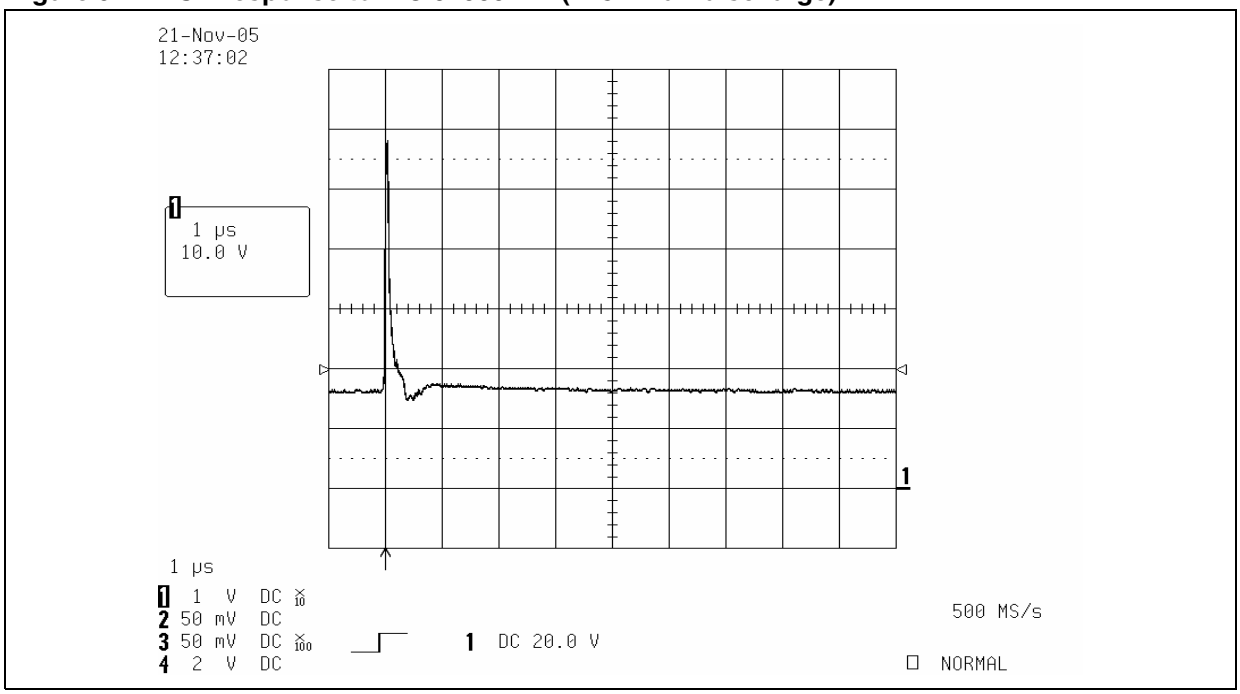


Figure 10. ESD response to IEC 61000-4-2 (-15 kV air discharge)

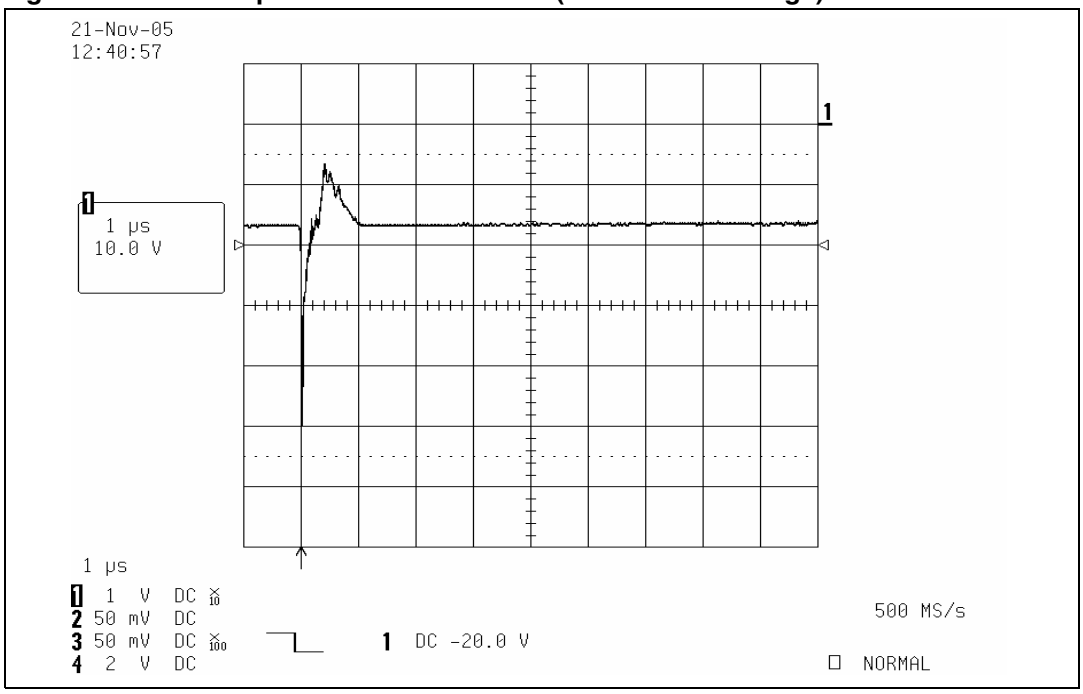
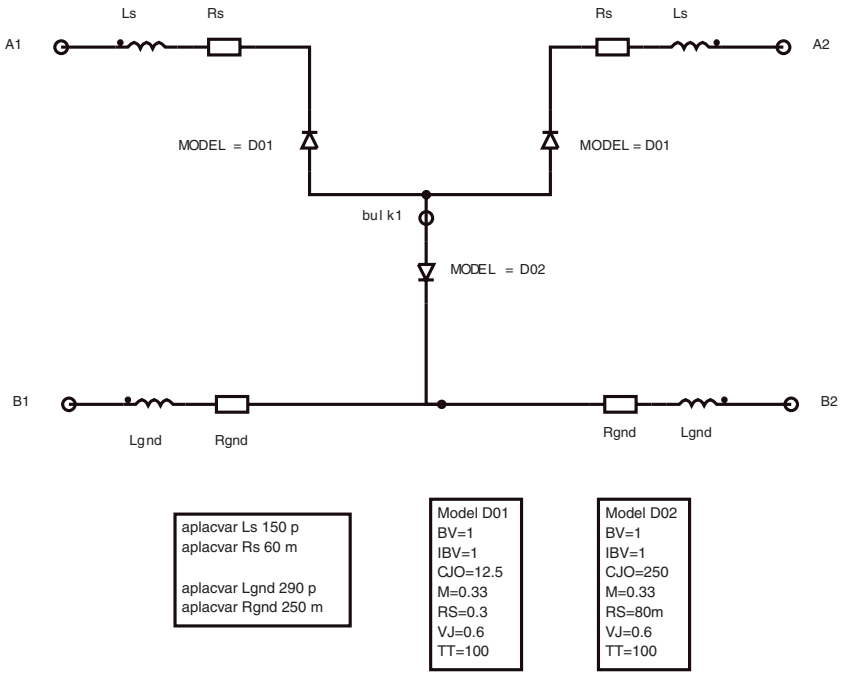


Figure 11. Digital crosstalk measurement

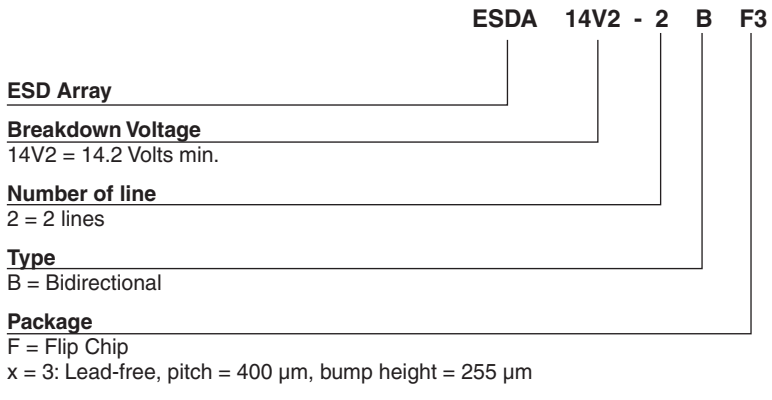
2 Application information

Figure 12. Aplac model



3 Ordering information scheme

Figure 13. Ordering information scheme



4 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at *www.st.com*.

Figure 14. Package dimensions

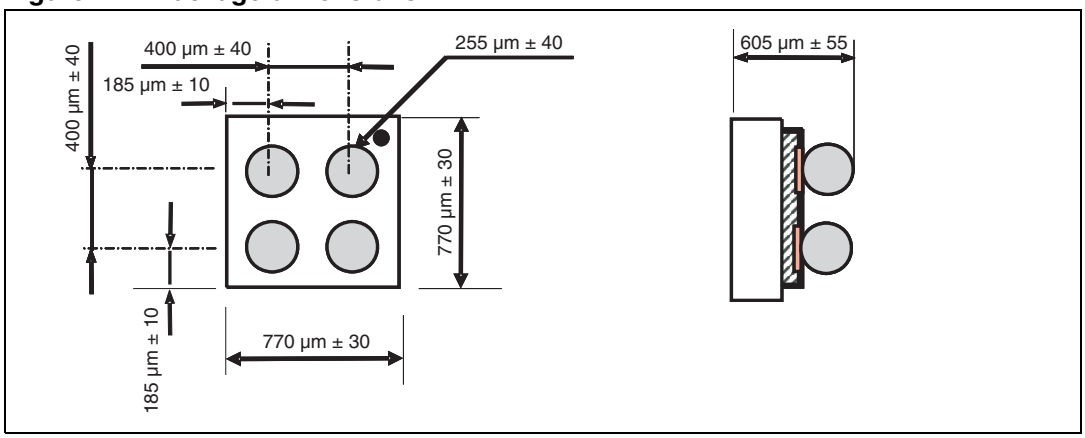


Figure 15. Footprint

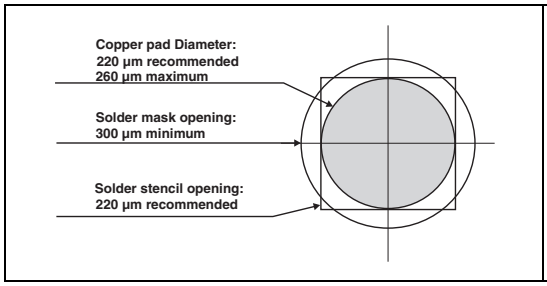


Figure 16. Marking

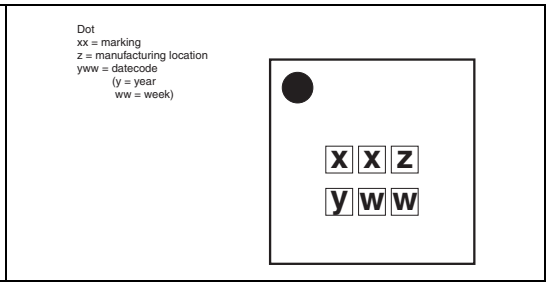
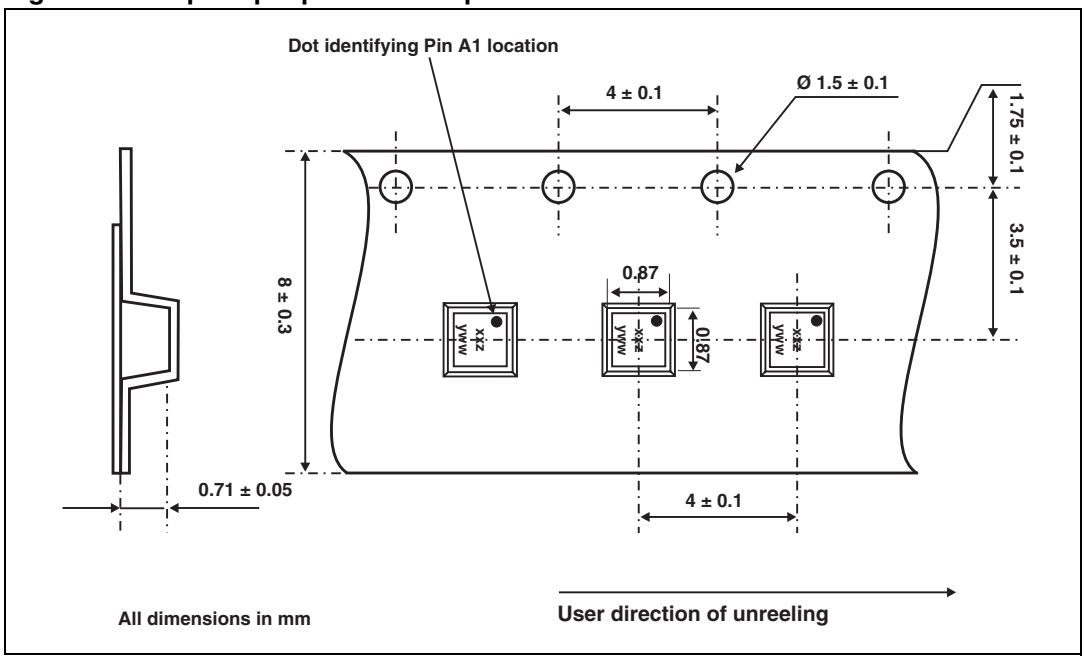


Figure 17. Flip Chip tape and reel specifications



Note: More information is available in the application note:
AN2348 :"400 µm Flip Chip: Package description and recommendations for use"
AN1751 : EMI Filters: Recommendations and measurements

5 Ordering information

Table 3. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
ESDA14V2-2BF3	EG	Flip Chip	0.79 mg	5000	Tape and reel 7”

6 Revision history

Table 4. Document revision history

Date	Revision	Changes
02-Dec-2005	1	Initial release.
15-Dec-2005	2	Ordering information changed.
29-Apr-2008	3	Updated ECOPACK statement. Updated *Figure 13* and *Figure 17.* Reformatted to current standards.

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