Ordering number : ENA0691

SANYO Semiconductors
DATA SHEET

LV5608LP — Bi-CMOS LSI For CCD Charge pump power supply

Overview

The LV5608LP is charge pump power supply for CCD.

Functions

- The charge pump boosts the +3.3V input by multiplying with +6, then by -3 to regulate the voltage to the specified level.
- The output voltage is +15V, -7.5V necessary for CCD.
- Soft start function incorporated, which reduces the inrush current at start of charge pump.
- Short-circuit protection function incorporated.
- Four types of operating frequency selectable.

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{DD} max		3.5	V
Allowable power dissipation	Pd max	with specified substrate *1	0.8	W
Operating temperature	Topr		-20 to +80	°C
Storage temperature	Tstg		-40 to +125	°C

*1 : Specified substrate : 40×50×0.8mm^3, glass epoxy four-layer (2S2P) board

Allowable Operating Ratings at Ta = 25°C, PGND = 0V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply voltage	V_{DD}		3.0	3.3	3.45	V
Input CLK frequency	CKIN	SEL=H *2	0.1		8	MHz
Input High voltage	$V_{IN}H$	EN pin	0.7V_{DD}		V_{DD}	V
Input Low voltage	$V_{IN}L$	EN pin	-0.1		0.4	V

*2 : Note that the charge pump frequency should be adjusted with S0/S1 so that it becomes 2 MHz or less.

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Electrical Characteristics at Ta = 25°C, V_{DD} = 3.3V, SGND = 0V, PGND = 0V,IH=20mA, IL=5mA, S0=H, S1=L, Unless otherwise specified

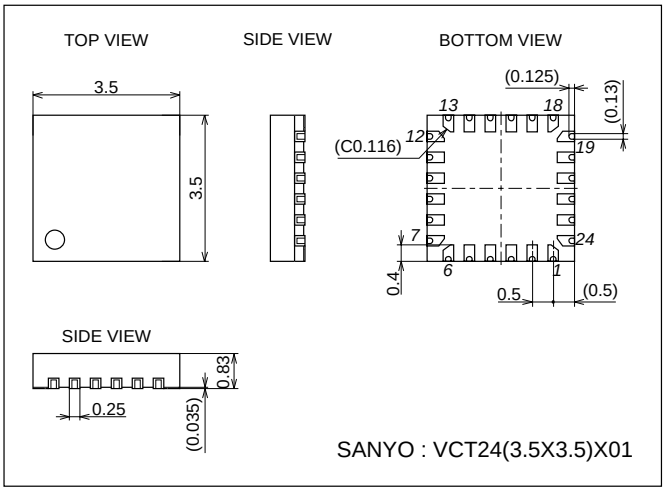
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Circuit current dissipation	$I_{DD}1$	EN = L		15	30	μA
	$I_{DD}2$	EN = H no load		17	25	mA
VH output load current	IH ave	V_{DD} = 3.0V			20	mA
VL output load current	IL ave	V_{DD} = 3.0V	-8			mA
Reference voltage	VREF	V_{DD} = 3.0 to 3.45V, design guarantee		1.305		V
		Ta = -20°C to +80°C, design guarantee	1.239		1.37	V
Output voltage accuracy	VH		14.55	15	15.35	V
	VL		-7.65	-7.5	-7.25	V
Output voltage at OFF	VOFF	After capacitive discharge	-50	0	50	mV
VH holding time	Toff	VLoff → VHoff	4.5	5.6	7.5	ms
Protection circuit masking time	Tmask		12	18	32	ms
VH load regulation	ΔVH	Load 1mA → 20mA		20	30	mV
VL load regulation	ΔVL	Load 0.5mA → 8mA		10	55	mV
Input pin current	Iin	Pins EN, S0, S1, SEL and CLK	12.6	17.5	22.5	μA
VH monitoring voltage	VTvlon			10		V
Power efficiency	Peff	CP+Regulator (VH+VL)		70		%
Inrush current	Irush				600	mA
Oscillation frequency	f clk		1.5	2	2.5	MHz

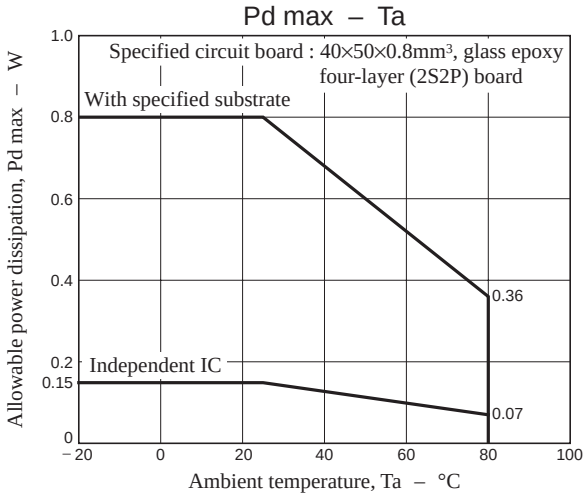
Note : The design specification items are design guarantees and are not measured.

Package Dimensions

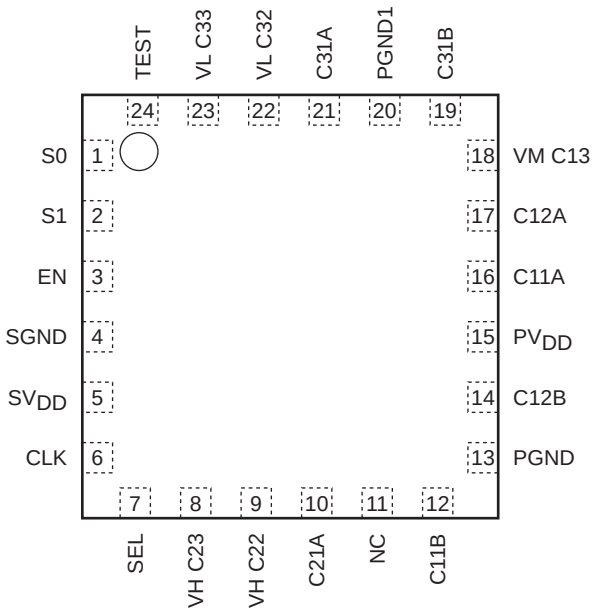
unit : mm (typ)

3322





Pin Assignment

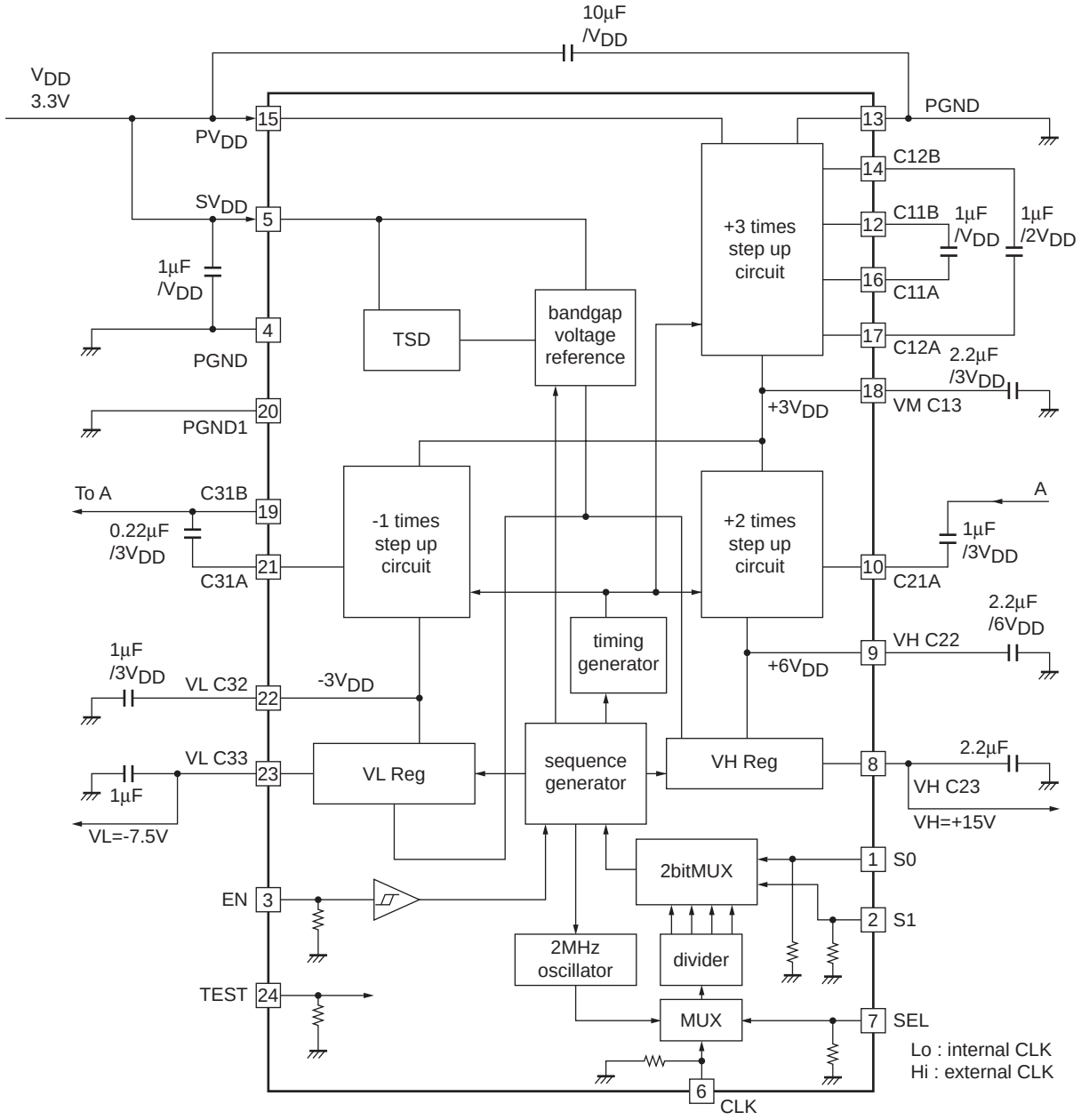


Top view

Pin Function

Pin No.	Name	Mode
1	S0	Charge pump frequency changeover pin
2	S1	Charge pump frequency changeover pin
3	EN	System enable pin (Hi active)
4	SGND	Small signal system GND pin
5	SV_{DD}	Small signal system V_{DD} pin
6	CLK	External CLK input pin
7	SEL	CLK selector pin (L: built-in CLK, H: external CLK)
8	VH C23	VH (+15V) regulator output pin
9	VH C22	Boost voltage output (+6V_{DD})
10	C21A	Boost capacitor connection pin (on the load transfer side)
11	NC	
12	C11B	Boost capacitor connection pin (driver side)
13	PGND	+3-fold boost power GND pin
14	C12B	Boost capacitor connection pin (driver side)
15	PV_{DD}	Power system V_{DD} pin
16	C11A	Boost capacitor connection pin (load transfer side)
17	C12A	Boost capacitor connection pin (load transfer side)
18	VM C13	Boost voltage output (+3V_{DD})
19	C31B	+2-fold and -1-fold boost capacitor connection pin (driver side)
20	PGND1	+2-fold and -1-fold boost power GND pin
21	C31A	-1-fold boost capacitor connection pin (load transfer side)
22	VL C32	Boost voltage output (-3V_{DD})
23	VL C33	VL (-7.5V) regulator output pin
24	TEST	Test pin (OPEN or GND short-circuited)

Block Diagram



Short-circuit Protection

VH and VL output pins incorporate the short-circuit protection function.
When the output pins are short-circuited to allow the large current to flow, IC is latched OFF to interrupt output.
To reset from the interrupted state, set the EN pin to L, then reset it again to H.

Frequency Selection

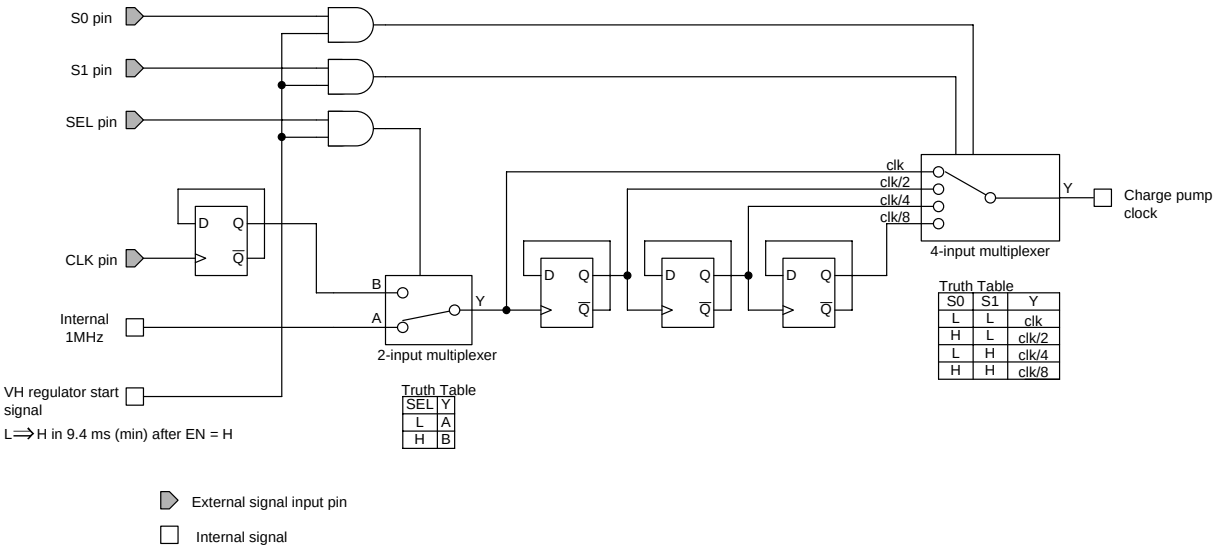
The charge pump operating frequency can be changed with S0 and S1 logics.
For light load, the reactive load can be reduced by lowering the operating frequency.
SEL logic also enables synchronous operation with external CLK.
The charge pump is operated with the frequency equivalent to 1/2 of input CLK.
(The IC internal oscillator is used for the sequence, so that it is normally ON regardless of SEL.

S0	S1	CP operating frequency	
		SEL=L	SEL=H
L	L	1MHz	1/2 CLK
H	L	500kHz	1/4 CLK
L	H	250kHz	1/8 CLK
H	H	125kHz	1/16 CLK

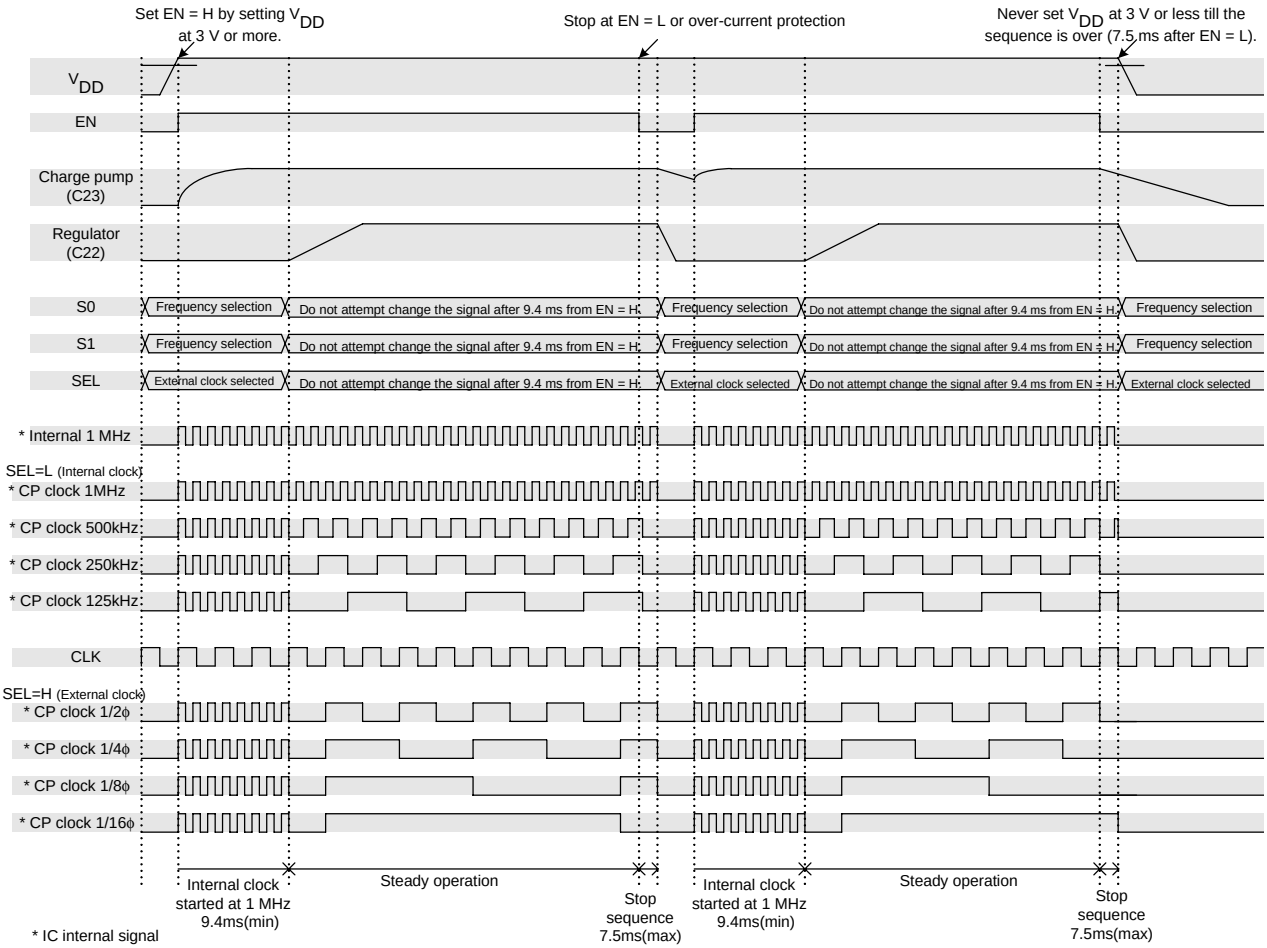
For minimum 9.4ms after startup with the EN signal set to H, the IC internal clock is used to operate the charge pump with 1 MHz regardless of the input of SEL, S0, and S1 pins. After the 9.4ms(min) period, the charge pump frequency is changed over according to the state of SEL, S0, and S1 pins. The changeover frequency is set as shown in the table right.

SEL	
L	IC internal oscillator
H	Synchronous operation with external CLK

Internal Equivalent Circuit



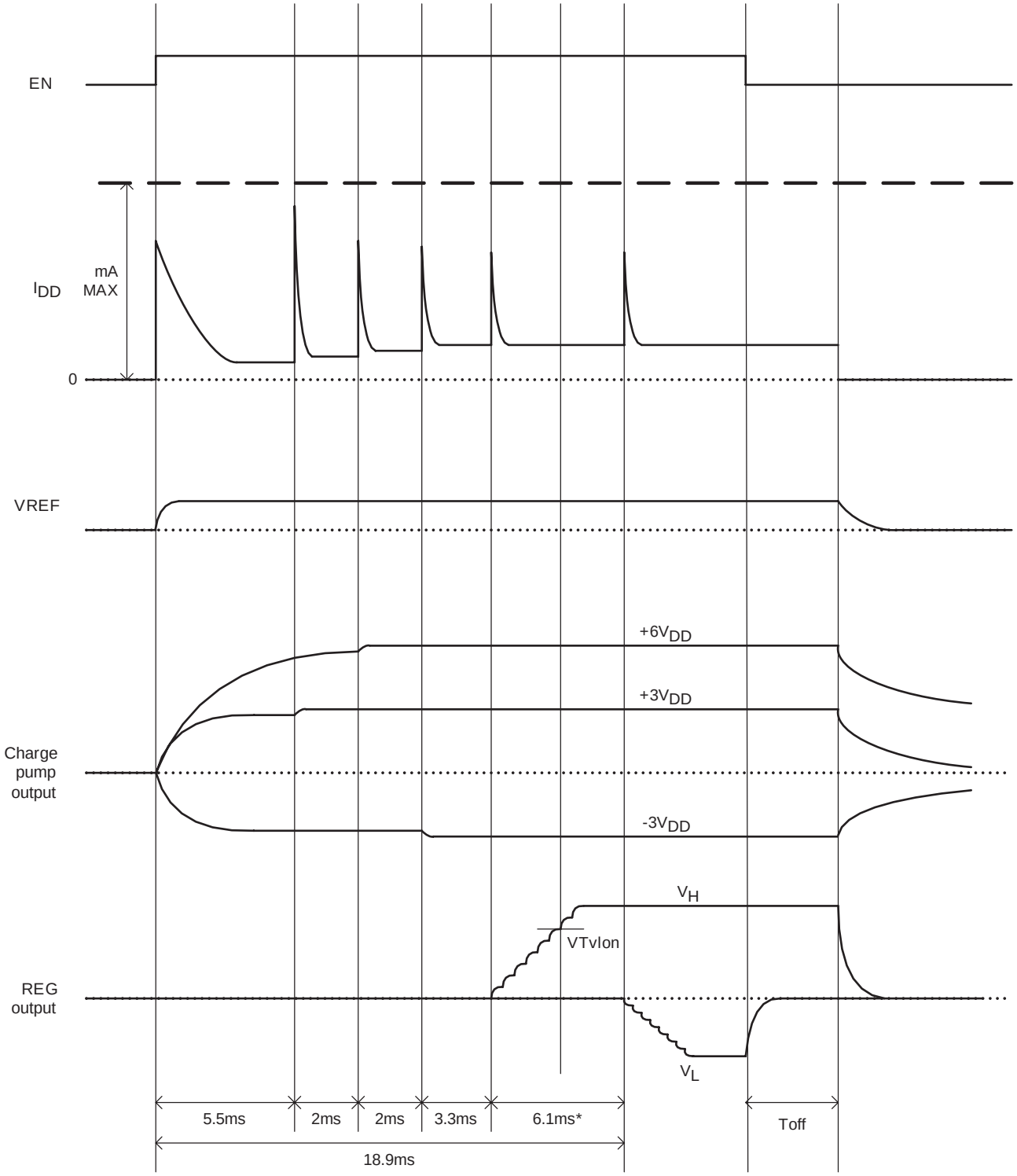
External clock signal startup sequence



EN Pin and V_{DD}

Though the sequence operation is made at startup, startup is not effectuated if the internal circuit has not been reset.
To reset the internal circuit, it is necessary to keep the EN pin at L till V_{DD} becomes 3V or more.
Note that operation with V_{DD} and EN pin short-circuited cannot be made.
Since the sequence operation is incorporated for stop of operation, the charge pump remains active till 7.5ms (max) passes after setting the EN pin to L. During this period, V_{DD} must be kept at 3V or more to allow the internal sequence logic to operate correctly.

Rise/fall Sequence



*The VL startup time at VH ≥ 10V and after elapse of 6.1ms is the reference time for CLK = 2MHz.